BK8000L Bluetooth Audio SoC Datasheet

Preliminary Specification

Approvals

Name	*Date*	*Signature*

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Revision History

Rev.	Date	Author(s)	Remark
0.1	10/May/2014	Weifeng	Initial Draft
0.2	5/June/2014	Weifeng	Add 7x7 56-pin package to support SD-card
	16/July/2014	Weifeng	Release the word file to XZX

Contents

1. General Description

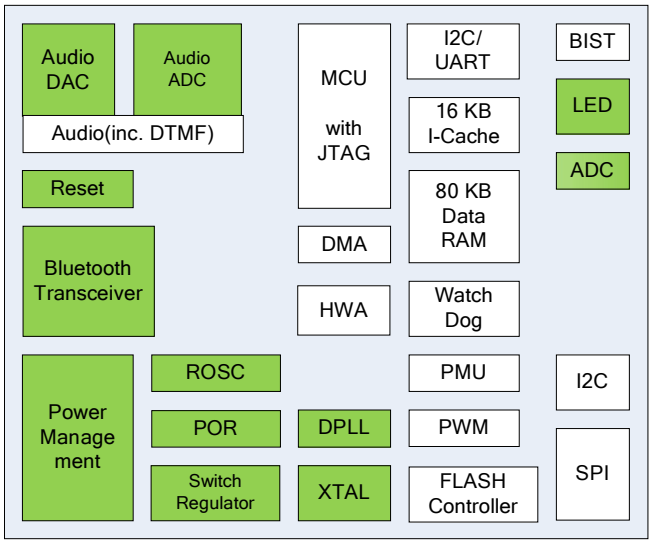
The BK8000L chip is a highly integrated single-chip Bluetooth audio device. It integrates the high-performance transceiver, rich features baseband processor, and Bluetooth audio profile. The BK8000L cache based architecture enables it is fully programmable with any application, that it may be used for control and multimedia hybrid application. The internal dual stereo ADC converts the stereo line in input to digital audio that enables the line in use the digital equalizer. Hardware equalizer and accelerator offload the MCU, and make it suitable for low power headset application.

1.1. Features

- Operation voltage from 2.8 V to 4.2 V
- Bluetooth 2.1+EDR compliant
- -92 dBm sensitivity for 2 Mbps mode and 5 dBm transmit power
- A2DP v1.2, AVRCP v1.0 and HFP v1.5 profile
- Integrated 96 dB SNR stereo ADC and stereo DAC
- Five bands hardware equalizer
- Digital equalizer for stereo line in
- Hardware accelerator for low power
- Full duplex hands-free speakerphone
- Up to 250 mA charge controller

1.2. Applications

- Bluetooth stereo speaker
- Bluetooth stereo headset
- Bluetooth control and multimedia hybrid



2. Pin Definition

It provides maximum QFN6x6 48-pins package for wireless audio application.

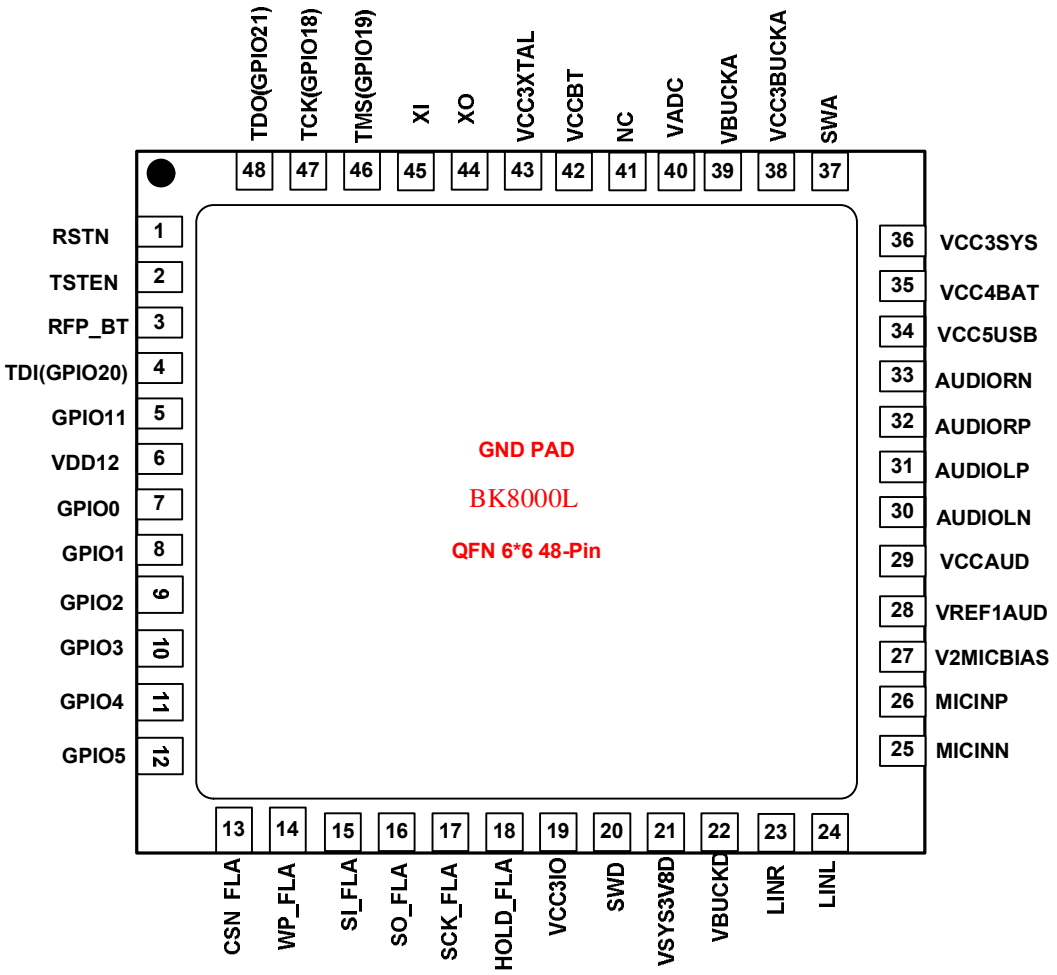


Table 1 Pin Description of 48Pin Package

PIN	Name	Pin Function	Description
1	RSTN	Digital I/O	Active low reset
2	TSTEN	Digital I/O	Test enable, high enable chip in test mode
3	RFP_BT	RF port	2.4 GHz antenna port
4	TDI	Digital I/O	JTAG TDI, GPIO20
5	GPIO11	Digital I/O	General I/O
6	VDD12	Power	1.2 V LDO output
7	GPIO0	Digital I/O	GPIO
8	GPIO1	Digital I/O	GPIO
9	GPIO2	Digital I/O	GPIO

10	GPIO3	Digital I/O	GPIO
11	GPIO4	Digital I/O	GPIO
12	GPIO5	Digital I/O	GPIO
13	CSN_FLA	Digital I/O	FLASH CSN
14	WP_FLA	Digital I/O	FLASH WP
15	SI_FLA	Digital I/O	FLASH SI
16	SO_FLA	Digital I/O	FLASH SO
17	SCK_FLA	Digital I/O	FLASH SCK
18	HOLD_FLA	Digital I/O	FLASH HOLD
19	VCC3IO	Power	3.3 V LDO output
20	SWD	Analog	Switch regulator port for digital
21	VSYS3V8D	Power	Input Power 3.6V
22	VBUCKD	Power	Switch regulator output for digital
23	LINR	Analog	Line in right channel
24	LINL	Analog	Line in left channel
25	MICINN	Analog	Microphone input negative
26	MICINP	Analog	Microphone input positive
27	V2MICBIAS	Analog	Audio bias voltage output
28	VERF1AUD	Analog	Audio reference output,1.2V
29	VCCAUD	Power supply	Audio power supply input, 1.8V~3.6
30	AUDIOLN	Analog	Audio left channel output negative
31	AUDIOLP	Analog	Audio left channel output positive
32	AUDIORP	Analog	Audio right channel output negative
33	AUDIORN	Analog	Audio right channel output positive
34	VCC5USB	Power	USB power input
35	VCC4BAT	Power	Battery input
36	VCC3SYS	Power	3.6V system LDO output
37	SWA	Analog	Switch regulator port for analog
38	VCC3BUCKA	Power	Switch regulator input for analog
39	VBUCKA	Power	Switch regulator output for analog
40	VADC	Analog	Battery detector ADC input
41	NC	NC	NC
42	VCCBT	Power	BT power supply input, 1.8V~3.6
43	VCC3XTAL	Power	XTAL power input, 3.6V
44	XO	Analog	XTAL output
45	XI	Analog	XTAL input
46	TMS	Digital I/O	JTAG TMS
47	TCK	Digital I/O	JTAG TCK
48	TDO	Digital I/O	JTAG TDO

3. Functional Description

3.1. GPIO

The BK8000L has total 19 GPIOs, which can be configured as either input or output. Most of them have second function.

Table 2 GPIO Function Mapping

功能分类	Mbist Mode	Perial Mode	GPIO Mode
GPIO0	Mbist Done	UART2_TXD/I2C2_SCL	General I/O
GPIO1	Mbist_Fail	UART2_RXD/I2C2_SDA	General I/O
GPIO2	input	pcm2_clk/TXEN	General I/O
GPIO3	input	pcm2_sync/RXEN	General I/O
GPIO4	input	pcm2_din/UART1_TX_Monitor	General I/O
GPIO5	input	pcm2_dout/UART1_RX_Monitor	General I/O
GPIO6	input	pcm2_codec_clk/spi_csn	General I/O
GPIO7	input	spi_sck	General I/O
GPIO8	input	spi_mosi	General I/O
GPIO9	input	spi_miso	General I/O
GPIO10	input	PWM0	General I/O
GPIO11	Mbist_Pass	PWM1	General I/O
GPIO12	input	sd_clk/clk13m	General I/O
GPIO13	input	sd_cmd/SCL	General I/O
GPIO14	input	sd_data[0]/SDA	General I/O
GPIO15	input	sd_data[1]	General I/O
GPIO16	input	sd_data[2]	General I/O
GPIO17	input	sd_data[3]	General I/O
GPIO18	Mbist_Fail_BT	jtag_TCK（上电默认）	General I/O
GPIO19	dram_result[2]	jtag_TMS（上电默认）	General I/O
GPIO20	dram_result[1]	jtag_TDI （上电默认）	General I/O
GPIO21	dram_result[0]	jtag_TDO（上电默认）	General I/O

All GPIO can be source to wake up MCU from shut down state. In shut down state, any level change on the set GPIO will trigger the wake up procedure.

When power on, the default state of GPIO0~GPIO9 and GPIO12~GPIO20 is high impedance and pull low internally; the default state of GPIO10~GPIO11 is high impedance and pull high; and the default state of GPIO21 is high impedance only.

3.2. PWM Timer and Watch Dog Timer

There are two sets of PWM timers. One fast set uses 1 MHz clock as main clock, and another slow set uses 32 kHz clock as main clock. Each set has three 16 bits counter with 4 bit pre-divider. First two timers in slow set can be used to LED duty cycle control.

The watch dog timer runs with 32 kHz clock, with period from 0.6 ms to 38 second.

3.3. Power Management

The BK8000L supports USB power supply that it can work without battery. When there is a USB power supply, it will charge the battery with automatically charge current control while provide power to the BK8000L. The buck will give nearly half current reduction for digital power.

The BK8000L can enter into shut down mode when there is no active connection. The shut mode can be waked up by GPIO and USB charge.

3.4. MCU

The 16 bit RISC MCU has 16 KB I-Cache and DMA bus, to support efficient execution and frequently data exchange. The JTAG interface can be used to on-line debug, which can be also configured as GPIO.

Besides 26 MHz crystal, the MCU can run with internal programmable ROSC clock, or 32 kHz ring oscillator clock, with programmable divided ratio.

3.5. I2C and UART Interface

There is one set of I2C interface and one set of UART interface for debug or external MCU control the BK8000L. They share the two same GPIO0 and GPIO1.

3.6. FM Receiver Control Interface

The FM receiver control interface consists of a two-wire I2C interface and a 13 MHz clock for FM receiver reference.

3.7. FLASH Access Interface

The BK8000L MCU is running with the external FLASH program memory and the internal instruction cache. The external FLASH can be also used to store user data such as key configuration and Bluetooth paring information.

3.8. SPI

The 4-wires SPI supports high speed data communication, which can be used as interface to either external FLASH or LCD controller.

3.9. SAR ADC and LED

The SAR ADC has 10-bit resolution, and the two LED drivers support up to 10 mA current.

The SAR has six active channel as follows.

Table 3 ADC Channel Table

Channel Number	Detected Voltage	Description
1	VBAT-pin/4	Battery voltage
2	VADC-pin	Pin VADC voltage
3	Charge current detector	Used to detect charge current and charge circuit control
4	VCC5USB-pin/6	USB voltage
5	GPIO19	GPIO19 voltage
6	GPIO9	GPIO9 voltage

3.10. Audio Peripheral

There are one set of speech ADC with sample rate 8 kHz or 16 kHz, 44.1 kHz or 48 kHz. The DAC have two channels for stereo application, with sample rate 8 kHz, 16 kHz, 44.1 kHz or 48 kHz.

There is also a stereo line in interface, to allow external stereo input passing internal 31 dB programmable gain amplify to stereo output.

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Parameter	Description	MIN	TYP	MAX	Unit
VCCBAT	Battery regulator Supply voltage	-0.3	3.3	4.2	V
P_{RX}	RX input power	-	10	-	dBm
T_{STR}	Storage temperature range	-40	-	150	℃
VCCIO	IO interface voltage	-0.3	2.8	3.6	V

4.2. Recommended Operating Conditions

Parameter	Description	MIN	TYP	MAX	Unit
VCCBAT	Battery regulator Supply voltage	2.8	3.3	4.2	V
T_{OPR}	Operation temperature range	-20	-	80	℃
VCCIO	IO interface voltage	1.8	-	4.2	V

4.3. System LDO

State	Description	MIN	TYP	MAX	Unit
VCC4BAT	VBAT	2.8		4.2	V
VCC3SYS	SYSLDO Output Voltage	2.8	3.6	3.8	V
Load Current	Loading Current			150	mA

4.4. Analog LDO/BUCK

System can choose the analog BUCK or LDO as the power supply of RF and Audio part.

State	Description	MIN	TYP	MAX	Unit
Analog LDO					
VCC3BUCKA	Analog LDO Input Voltage	2.8	3.3	3.6	V
VBUCKA	Analog LDO Output Voltage	1.7	1.8	2.4	V
Load Current	Loading Current			100	mA
Analog BUCK					
VCC3BUCKA	Analog BUCK Input Voltage	2.8	3.3	3.6	V
VBUCKA	Analog BUCK Output Voltage	1.7	1.8	2.4	V
Load Current	Loading Current			100	mA
Switching frequency	BUCK modulation frequency	2	5	10	MHz

4.5. Digital LDO/BUCK

System can also choose the digital BUCK or LDO as the power supply for the Digital part.

State	Description	MIN	TYP	MAX	Unit
Digital LDO					
VSYS3V8D	Digital LDO Input Voltage	2.8	3.3	3.6	V
VBUCKD	Digital LDO Output Voltage		1.2	1.35	V
Load Current	Loading Current			100	mA
Digital BUCK					
VSYS3V8D	Digital BUCK Input Voltage	2.8	3.3	3.6	V
VBUCKD	Digital BUCK Output Voltage		1.2	1.35	V
Load Current	Loading Current			100	mA
Switching frequency	BUCK modulation frequency	2	5	10	MHz

4.6. USB LDO

When USB is plug in, VCC3SYS will be generated from USB LDO.

State	Description	MIN	TYP	MAX	Unit
VCC5USB	USB Input Voltage	4.75	5	5.75	V
VCC3SYS	USBLDO Output Voltage		3.3		V
Load Current	Loading Current			100	mA

4.7. Typical Power Consumption

State	Description	MIN	TYP	MAX	Unit
Shut down	Software shut down, wake up from GPIO		50		uA
Idle-Sniff	Idle state at Sniff mode		900		uA
Active (A2DP)	2DH5		20		mA
Active (HFP)	HV1		20		mA

4.8. RF Characteristics

Parameter	Condition	MIN	TYP	MAX	Unit
Operate Frequency	2402~2480	2402		2480	MHz
RXSENS-1 Mbps	BER=0.001		-90		dBm
RXSENS-2 Mbps	BER=0.0001		-92		dBm
RXSENS-3 Mbps	BER=0.0001		-84		dBm
Maximum received signal	BER=0.001	0			dBm
Maximum RF transmit power			5		dBm
RF Power Control Range		30			dB

4.9. Audio Characteristics

Parameter	Condition	MIN	TYP	MAX	Unit
DAC Output Amplitude				1	Vrms
DAC output SNR	1 kHz sine wave		96		dB
DAC Sample Rate		8		48	kHz
ADC SNR	1 kHz sine wave		96		dB
ADC Sample Rate		8		48	kHz

5. Application Schematic

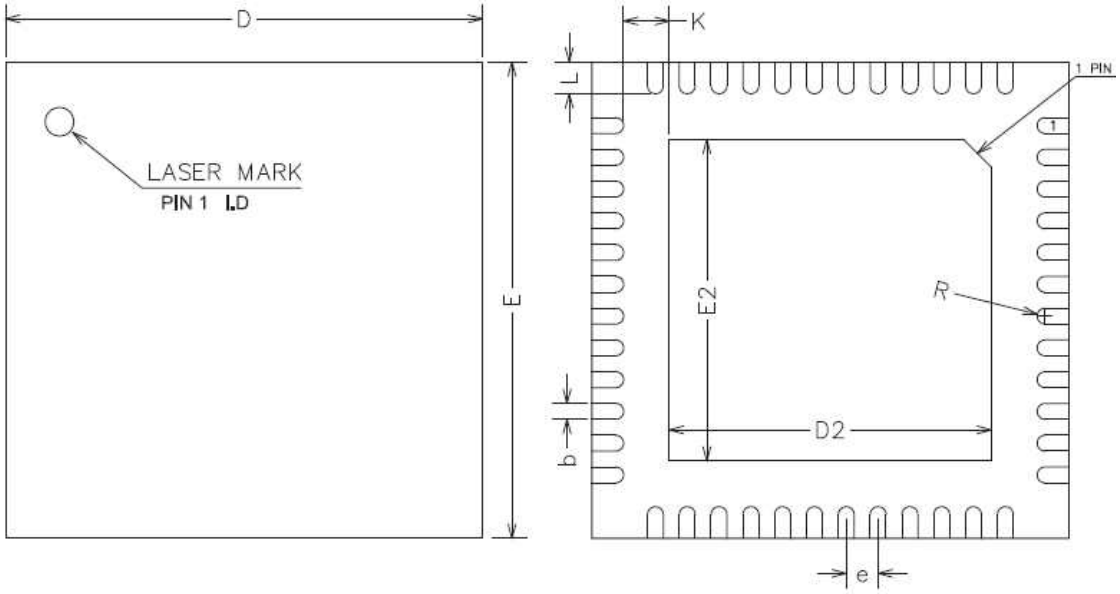
It will be provided with separate document.

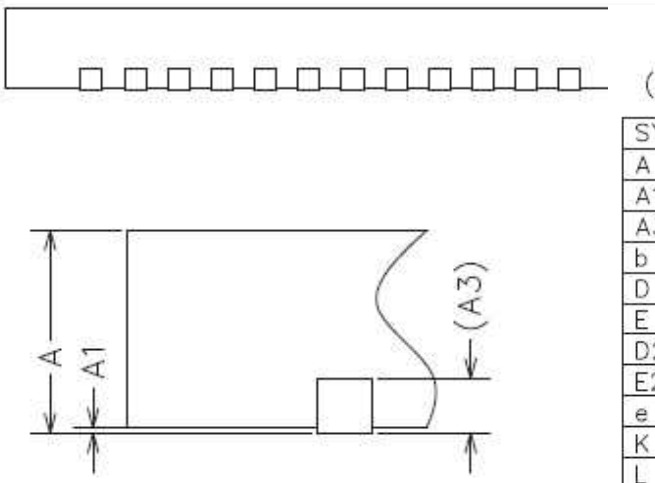
6. About the Qualification

By carefully PCB layout, the BK8000L RF performance meets FCC, CE and BQB requirement. The Bluetooth protocol and profile provided by Beken are already qualified and listed in SIG website. If there is any end product listing requirement with the BK8000L, please inquire Beken for the related QDID authorization.

7. Package Information

The BK8000L uses the QFN 6x6 48-Pin package.





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–

8. Ordering Information

Part number	Package	Packing	MOQ (ea)
BK8000LQB	QFN 6mmx6mm 48-Pin	Tape Reel	10 k

Remark:

MOQ: Minimum Order Quantity